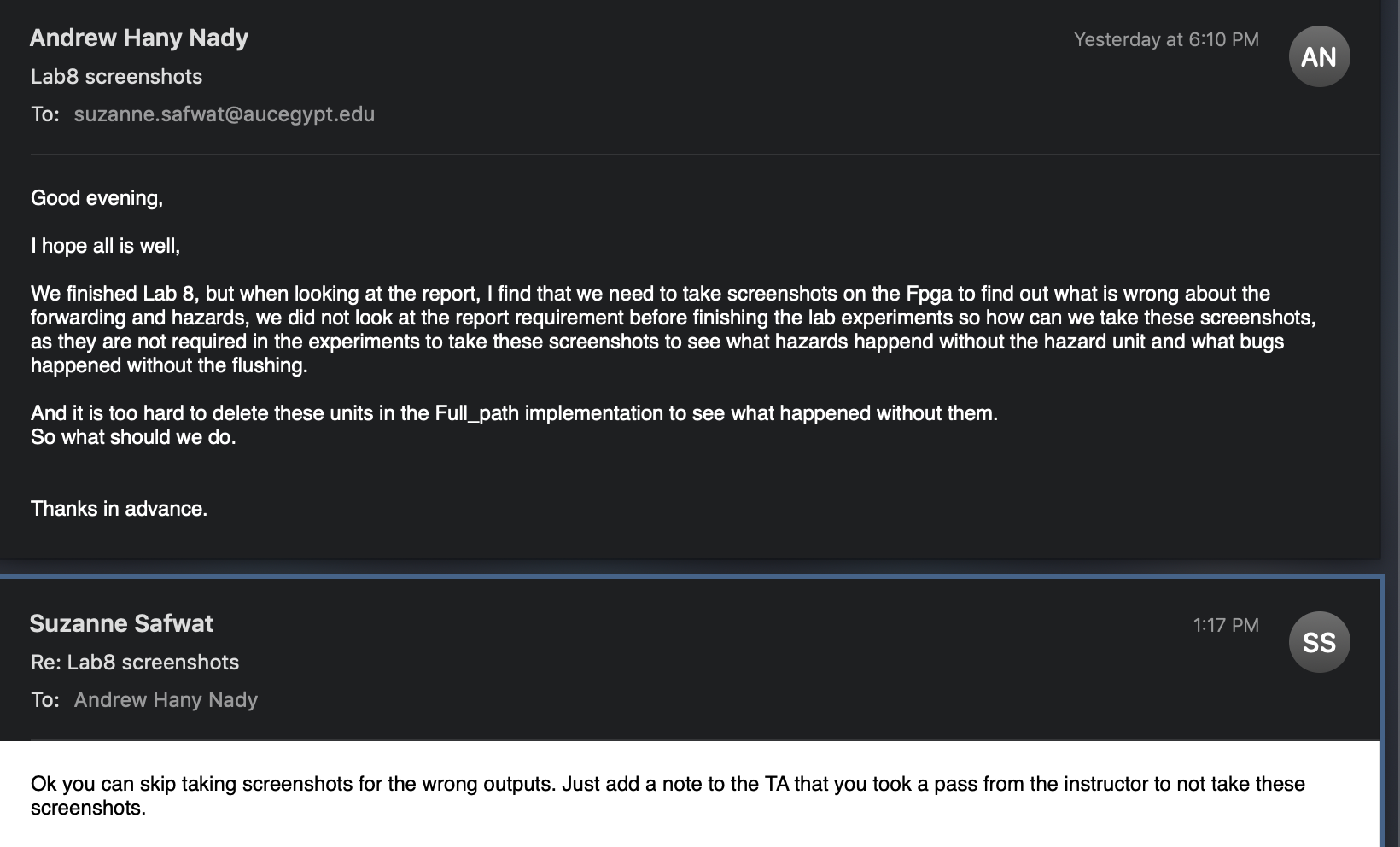
Lab 8

Andrew Nady

Question 2:

Code is provided in a separate file

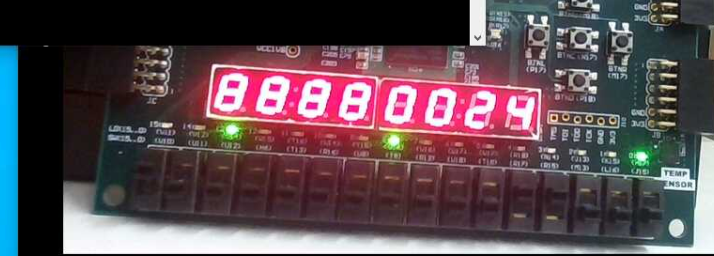
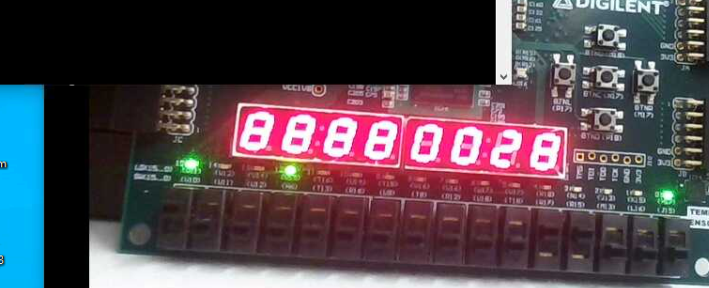
Question 3&4:

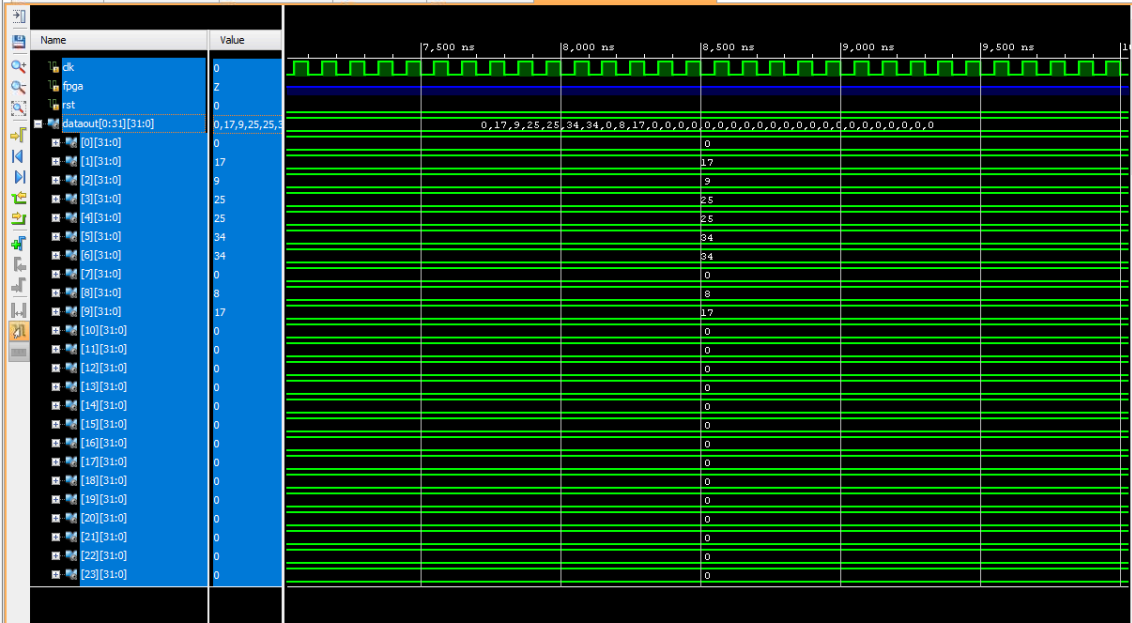
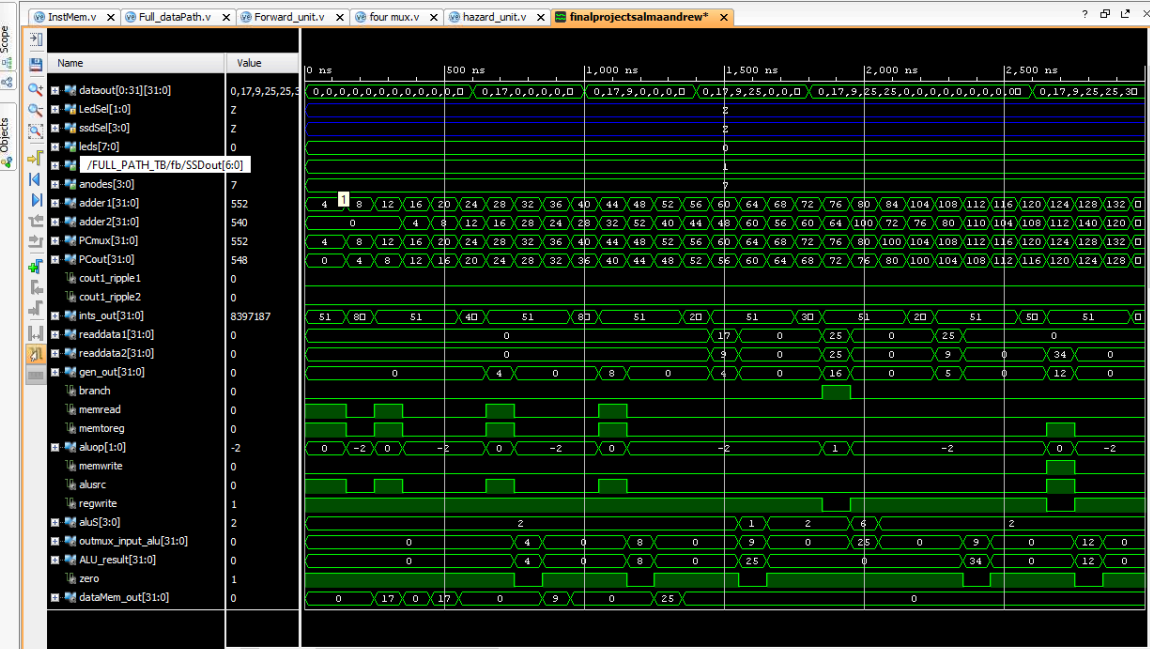
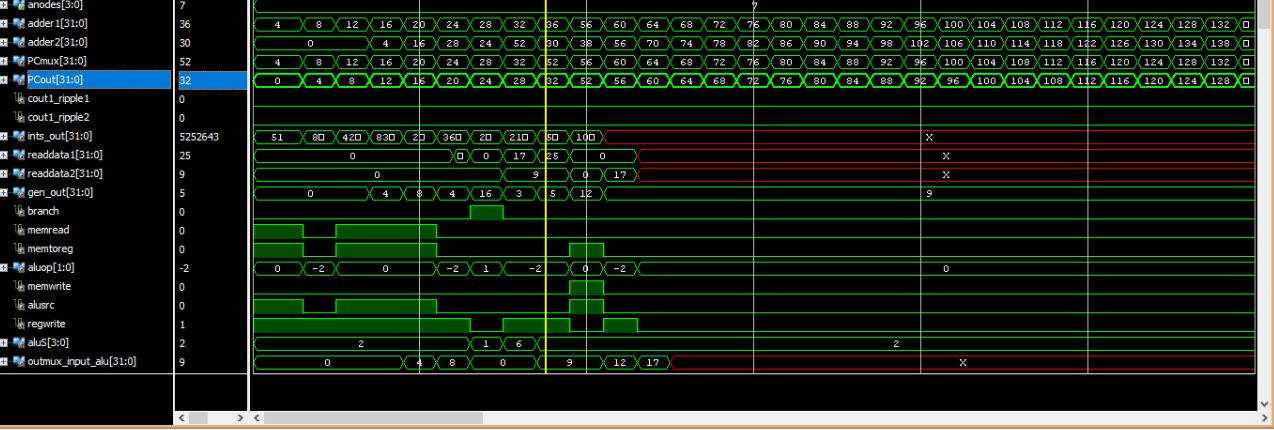
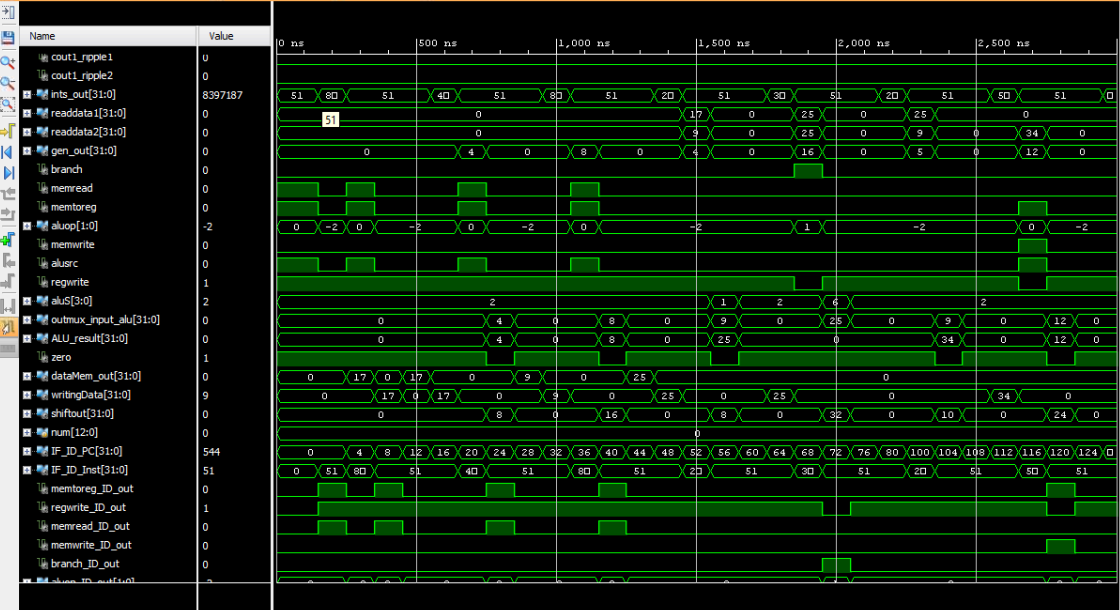


As we finished the lab before taking all the screenshots required, so we took a pass from the Doctor. However; we took some screenshot,

Experiment 2:

Here we are not expecting that the branches will work properly, as we only did the forwarding. But did not do the flushing yet. Here some screenshots on the FPGA and the simulation which has some issues in the branches.

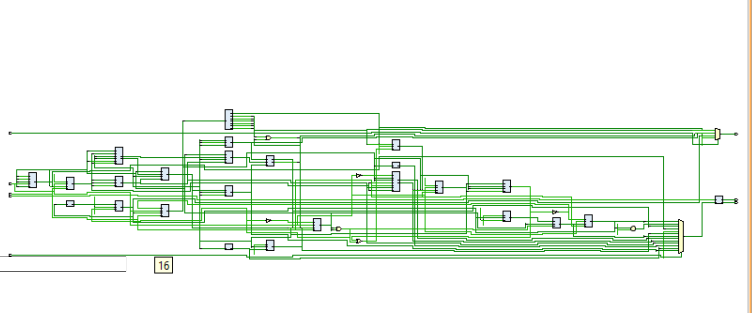


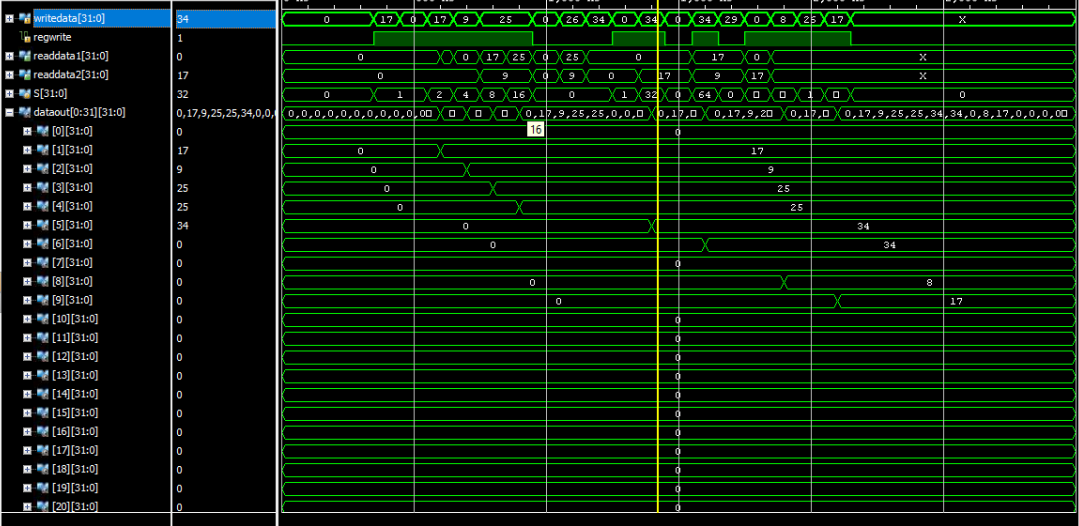


Experiment 3:

In this point, we have a processor which is totally functional in all cases, and can deal with all hazards (data, control)

The below screenshot of the simulation indicates that all the results are true as expected from the program





Question 5:

If we have hazards in the mem and ex stages, then we need to forward it form the ex-stage, as it is the most updated value where if the value in mem stage of X3 =3, and then we modified it the ex-stage to be equal to 6, then it is more logical to forward the EX stage values

Question 6:

(EX/MEM.RegisterRd ≠ 0): then means that rd =0 means that if the register not x0

That is because the register zero won’t be updates so we don’t need to forward it